Received 13 December 2024; revised 27 January 2025; accepted 28 January 2025. Date of publication 31 January 2025; date of current version 21 March 2025.
The review of this article was arranged by Editor A. S. Verhulst.

Digital Object Identifier 10.1109/JEDS.2025.3537290

Electrical and 850 nm Optical Characterization of Back-Gate Controlled 22 nm FDSOI PIN-Diodes Without Front-Gate

JELLE H. T. BAKKER [1,2] (Graduate Student Member, IEEE), MARCIN Ł. MOTYCKI [1,2] (Graduate Student Member, IEEE), RAYMOND J. E. HUETING [2] (Senior Member, IEEE), ANNE-JOHAN ANNEMA [1,2] (Member, IEEE), AND MARK S. OUDE ALINK [1,2] (Senior Member, IEEE)

1 Group of Integrated Circuit Design, University of Twente, 7522 NB Enschede, The Netherlands
2 Faculty of Electrical Engineering, Mathematics and Computer Science, University of Twente, 7522 NB Enschede, The Netherlands

CORRESPONDING AUTHORS: J. H. T. BAKKER AND M. Ł. MOTYCKI (e-mail: j.h.t.bakker@utwente.nl; m.l.motycki@utwente.nl)

The work of Jelle H. T. Bakker was supported in part by the Bruco Integrated Circuits and Holland High Tech in a Public–Private-cooperation for research and development in the Hightech Systems and Materials Topsector. The work of Marcin Ł. Motycki was supported by the European Union through the Horizon Europe Project Qu-PIC under Grant 101135845.
This paper was presented in part at the 50th IEEE European Solid-State Electronics Research Conference (ESSERC), September 2024.
DOI: https://doi.org/10.1109/ESSERC62670.2024.10719482.
(Jelle H. T. Bakker and Marcin Ł. Motycki contributed equally to this work.)

ABSTRACT We present electrical and optical ($\lambda = 850$ nm) measurement results of back-gate controlled SOI PIN-diodes without a front-gate, with an intrinsic Si film thickness of only ~6nm. These ultrathin-body PIN-diodes were fabricated as exploratory devices in a commercially available Fully-Depleted Silicon-On-Insulator (FDSOI) technology, without requiring additional process steps. We show that electrostatic back-gate tuning significantly affects the electrical characteristics and optical responsivity (R_o). This leads to a novel method to extract the optimal back-gate bias for maximum R_o from electrical measurements. The maximal measured R_o at 0V bias across the diode and with optimal back-gate bias equals 62μA/W, with a −3dB bandwidth of 5.9GHz, and a −6dB bandwidth of 15GHz. These PIN-diodes potentially open the way to new (THz) circuits, sensors, novel/complementary process control monitoring structures, and optical applications. They also enable interaction between the hybrid (bulk) and SOI devices, which is a unique feature of FDSOI technologies.

INDEX TERMS 22 nm FDSOI, 22FDX®, PIN-diode, SOI PIN-diode, photodiode, SOI PIN PD, 850 nm, back-gate control.

I. INTRODUCTION

Globalfoundries® Fully-Depleted Silicon-On-Insulator (FDSOI) technology includes an extensive array of possible devices on both hybrid (bulk CMOS) and SOI within the same technology [1] (1). The 22FDX® devices built on top of the buried oxide (BOX) offer great electrostatic control and minimum gate-induced drain leakage [1]. The active intrinsic silicon (Si) film is traditionally covered by a poly-Si High-K Metal Gate (HKMG) stack, acting as a front-gate. This front-gate is the main control terminal for field-effect devices, but for some applications, for example when the Si film would be used as the intrinsic (I)-part in an SOI PIN-diode, it can limit the electrical (*e.g.*, via additional parasitic capacitance) and optical (*e.g.*, by blocking light at the top surface) potential of the intrinsic Si film.

In this work, we present FDSOI PIN-diodes (1) without a front-gate. The presented devices have been fabricated as exploratory devices using engineering wafers in 22FDX®, *i.e.,* without any additional process steps. This means that these devices could potentially be fabricated in any technology that uses a similar process flow. In the remainder of this work, we use the name SOI-diode instead of FDSOI-diode to prevent any potential confusion with diodes made on hybrid (bulk) area in the FDSOI-technology platform.

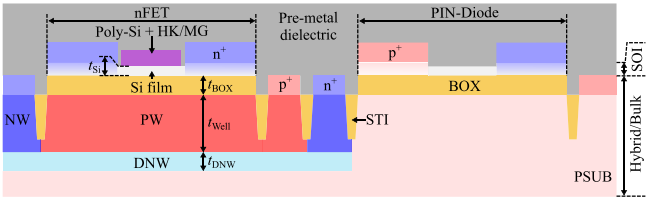


FIGURE 1. Cross-section of an SOI transistor, hybrid (bulk) pn-junctions, hybrid wells, and the novel SOI PIN-diode without a front-gate in 22nm FDSOI.

PIN-diodes are extremely versatile devices. For example, their fast reverse recovery phenomenon is a key element in THz pulse generators [2], frequency multipliers [3], and frequency dividers [4]. PIN-diodes are also used in voltage limiters [5], linear attenuators [6], [7], RF switches [8], and high-voltage applications [9]. Combining the reduced parasitic capacitance of the presented PIN-diodes with modern FDSOI transistors delivering superior RF performance and digital processing capabilities could result in very cost-effective and high-performance solutions. In this first iteration, however, we limit ourselves to the optical and DC electrical characteristics.

The 850nm wavelength is commonly used for optical communication, and the Si photodiode (PD) is a suitable photodetector at this wavelength [10]. Since the performance of the SOI PIN-diode depends on parameters like the SOI thickness (t_{Si}), interface quality, and doping, these structures can also be used for Process Control Monitoring (PCM). The absence of the HKMG is essential if these devices are used as PDs for optical process monitoring, which requires top-side wafer probing for high-volume manufacturing where low monetary and time costs are crucial. For more general optical applications, back-side illumination might be an option, but then the dies have to be backgrinded and the light will still (partially) be absorbed by the Si substrate making this an undesirable option.

In traditional vertical bulk Si PDs shorter wavelengths ($300 - 400$nm) are absorbed by the silicon above the depletion region, making them unable to function as photodetectors. However, there is no Si above the intrinsic Si film of the SOI PIN-diode. This makes it possible for them to perform as photodetectors for these shorter wavelengths [11]. Note that the ∼6nm thick Si film [12] of the PIN-diodes will limit the responsivity (R_o).

Combining bulk devices right below the SOI devices, as reported for Single Photon Avalanche Diodes (SPADs) [13] and back-gates (bulk wells plus BOX) [1], allows for the exploration of interactions between these bulk devices and PIN-diodes as demonstrated in this work. Back-gates in SOI technology have already been extensively used, for example, for tuning SOI FET's electrical performance [1], which is different from, *e.g.,* RF-SOI or PD-SOI where the BOX-layer as well as the SOI-layer are much thicker. The back-gate can be used to tune the charge carrier concentrations of the intrinsic Si film [14], [15], [16], [17] of the SOI PIN-diode. This is useful for improving and/or controlling electrical and optical properties like dark current and R_o [18].

Extending earlier work [19], we present additional extensive measurement results of SOI PIN-diodes without a front-gate in a commercial FDSOI process. Furthermore, we show and discuss the effect of electrostatic back-gate tuning on the charge carriers in the SOI PIN-diode that both affect the electrical characteristics and R_o. We introduce a novel method to obtain the back-gate bias for maximum R_o from purely electrical measurements. This can be leveraged to increase the R_o by an order of magnitude by setting an optimum back-gate bias voltage. This control of the R_o can also be used to compensate for, *e.g.,* process or temperature variations.

This paper is organised as follows: Section II explains the effect of the back-gate, Section III discusses the designed diode layouts, Section IV describes the experimental setups, Section V presents and discusses the electrical and optical measurement results, and in Section VI the main findings and conclusions are summarized.

II. ELECTROSTATIC BACK-GATE CONTROL

Conventional thin-film gated diodes have a current-voltage (I-V) dependency on both the front-gate and back-gate potential (V_{BG}) relative to the anode (V_P) and cathode (V_N) potential [14]. Our thin-film devices do not have a front-gate, see 2, leaving only the V_{BG} (PSUB) potential to affect the I-V characteristics. Throughout this work it is assumed that V_{BG}, V_N (n^+), and V_P (p^+) are defined as relative to a common ground.

Fig. 2 illustrates simplified cross-sections and energy band diagrams of the SOI PIN-diodes for various V_{BG} assuming no incident light. With the terminals p^+ and n^+ set to $V_P = V_N = 0$V, three scenarios are shown for different V_{BG} relative to $V_{BG,max,R}$. Here $V_{BG,max,R}$ is defined as the V_{BG} for which the PIN-diodes have a maximum R_o when $V_P = V_N = 0$V (as explained later in this section). At that V_{BG} the device behaves as an actual PIN-diode and, consequently, operates best as a PD for the given diode voltage.

Fig. 2(a) shows the charge carrier distribution and energy band diagram for $V_{BG} = V_{BG,max,R}$. In this case, there are hardly any charge carriers in the intrinsic region. For this V_{BG} the R_o will be maximum because the Si film has its maximum intrinsic Si volume. When an incident photon with $\lambda < 1100$nm [20] is absorbed in the Si film, an electron-hole pair is generated. Due to the electric field stemming from the built-in (lateral) potential, the generated charge carriers are quickly separated and drift towards the p^+ and n^+ regions, resulting in a photocurrent. For low forward voltages ($V_{PN} < 0.6$V), in the absence of light, the recombination current is the dominant current component. The Shockley-Read-Hall (SRH) recombination is highest in the regions where p is equal to n and the pn product is maximal [21]. For PIN-diodes this is the case in the intrinsic region; therefore, a maximum intrinsic Si volume results in a maximum recombination current. Consequently, for a

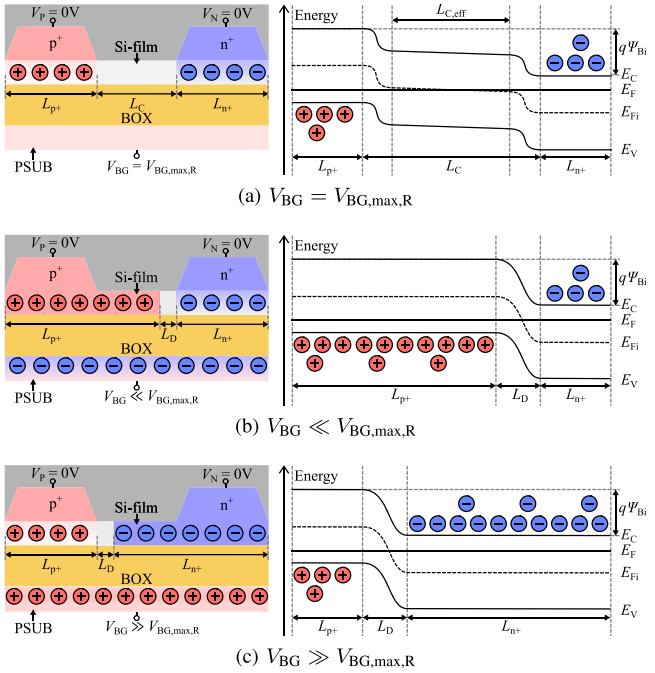


FIGURE 2. Schematic illustration of the electrostatic back-gate control in SOI PIN-diodes under dark condition. (left) Charge carrier distributions in the device, and (right) horizontal energy band diagrams for different V_{BG}.

given applied V_{PN} both the R_o and recombination current are maximum when $V_{BG} = V_{BG,max,R}$.

Differences in doping levels of the n^+ and p^+ regions as well as in the work functions of the SOI layer and the back-gate result in a $V_{BG,max,R}$ that is not exactly 0V. The finite Debye lengths cause long tails in the lateral direction in the energy bands from the level in n^+ and p^+ to the level in the intrinsic Si. The result is that the actual fully depleted part of the intrinsic region, $L_{C,eff}$, is smaller than L_C, as also shown in the figure.

Fig. 2(b) shows the charge carrier distribution and energy band diagram for $V_{BG} \ll V_{BG,max,R}$. In this scenario, the applied V_{BG} induces a negative charge under the BOX, which attracts holes in the Si film. Since the film is ultrathin, it can be assumed that (almost) all of its volume is now full of holes [22]. The large density of attracted holes effectively increases the (p-type) doping in the Si film, turning the PIN-diode into a PPN-diode with a relatively small depletion region (L_D). The electron-hole pairs generated outside of the narrow depletion region must now rely on slow diffusion instead of drift to be separated. This combined with the reduction of L_D and any (potential) defects in the top interface of the Si film effectively reduces R_o. Moreover, for high negative V_{BG} the ultrahigh hole concentration near the n^+ region could form a tunnel junction [15], which would lead to an increase of (tunnel) current.

Fig. 2(c) shows the charge carrier distribution and energy band diagram for $V_{BG} \gg V_{BG,max,R}$. This results in exactly the opposite to what is depicted in Fig. 2(b) resulting in a PNN-diode, thus the R_o is also expected to be significantly reduced. Similarly, an ultrahigh electron concentration could also form a tunnel junction, but then near the p^+ region.

We use the principle of the electrostatic back-gate control described above in our measurements, as discussed in Section V, to characterize the device and to obtain maximum R_o.

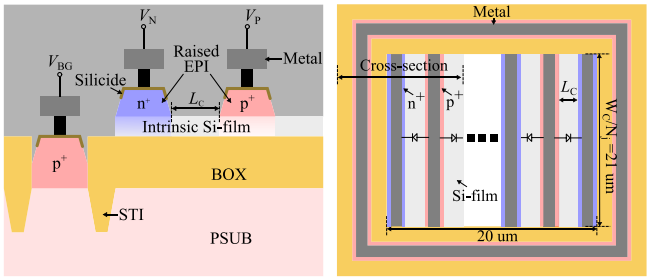


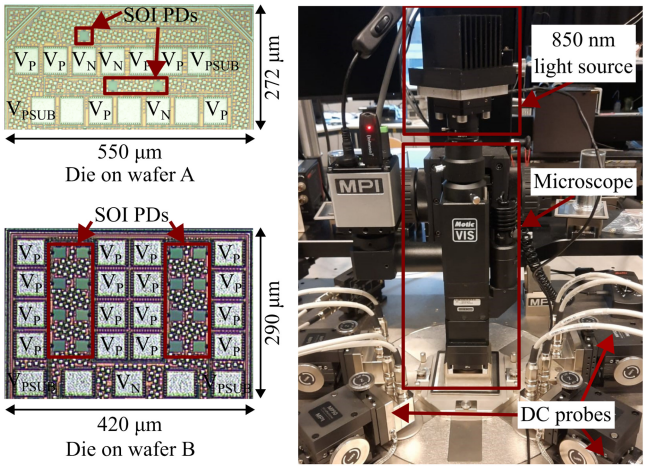
FIGURE 3. Schematic layout of the SOI PIN-diode without a front-gate: (left) cross-section, and (right) top view. Here N_j is the number of parallel PIN-junctions.

III. SOI PIN-DIODE LAYOUT

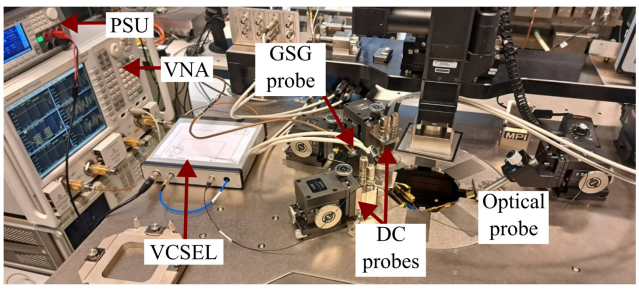
A schematic layout of the SOI PIN-diodes is shown in Fig. 3. Each device consists of several parallel-connected PIN-junctions, for characterisation sensitivity purposes. Devices were designed and fabricated with five different lengths of the intrinsic region (L_C): 157nm, 260nm, 527nm, 1090nm, and 2127nm. The total widths (W_C) of the parallel PIN-junctions are: $93.1 \cdot 10^{-3}$ cm, $71.9 \cdot 10^{-3}$ cm, $50.8 \cdot 10^{-3}$ cm, $29.6 \cdot 10^{-3}$ cm, and $16.9 \cdot 10^{-3}$ cm, respectively. These widths are used to report dimension-independent currents per unit width (A/cm). The area (including metal wiring) for all devices is $21\mu m \times 20\mu m$, which aligns with the typical beam sizes of fibre-coupled lasers. Metal coverage of the diodes (in the Back End Of Line (BEOL)) was minimised to reduce light blockage. The metal area has been subtracted from the device area when calculating R_o.

IV. EXPERIMENTAL SETUP

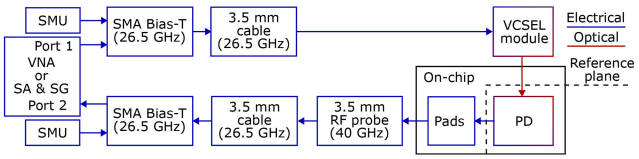
We studied devices from two 22FDX® wafers (A and B). Fig. 4(a) shows single dies containing test structures on wafers A and B respectively. Wafer A allows for RF measurements with a Ground-Signal-Ground (GSG) probe (FormFactor Infinity I40). Wafer B contains more device variants but only allows for DC measurements. All measurements were done on a probe station (MPI TS300-SE). *I-V* sweeps were measured with a semiconductor parameter analyser (Keithley 4200). R_o (A/W) (is explained in detail in Section V.D) measurements were done with a custom calibrated 850nm light source consisting of IR-LEDs (OSLON® 9 IR PowerClusters) followed by an optical 10nm filter (Thorlabs FBH850-10) (Fig. 4(b)). The frequency response measurements use a Vertical Cavity Surface Emitting Laser (VCSEL) (VI Systems V50-850M). The VCSEL's calibration data consists of S_{11} (measured



(a) Die micrographs. (b) Responsivity measurement setup.



(c) S-parameter measurement setup.



(d) Schematic block diagram of the frequency response measurement setups.

FIGURE 4. Die micrographs and measurement setups.

at the electrical input of the VCSEL) and $|S_{21}|$ (from the electrical input to the optical output power of the VCSEL. For the Device Under Test (DUT), the $|S_{21}|$ is from the optical input (port 1) to the electrical output (port 2) [23]. The VCSEL output is connected to a lensed fibre (Thorlabs LFM1F-1) that is aligned using a micromanipulator above the DUT.

The frequency (f) response was measured with two measurement setups (Fig. 4(d)). For measurements at $f >$ 0.5GHz, a Vector Network Analyser (VNA) (Keysight N5244A) was used (Fig. 4(b)) (port 1 of the VNA was calibrated up to the connector of the VCSEL). Port 2 of the VNA is connected to the GSG RF probe, which was calibrated using an Impedance Standard Substrate (ISS) (Cascade 101-190), and is connected to the on-chip pads. The signal needle of the GSG RF probe connects to the cathode (V_N) and both ground needles connect to the anode (V_P). The capacitance between the on-chip signal (pad and trace) and ground (pads and traces) was measured and de-embedded on a separate (open) de-embed structure.

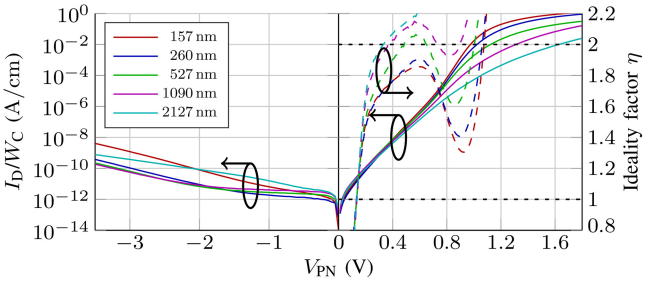


FIGURE 5. Gummel plot (drawn curves) and calculated ideality factor (dashed curves) as a function of V_{PN} of five PIN-diodes on the same reticle ($D_{4,3}$) on wafer B with $V_{BG} = V_{BG,max,R}$ and $V_P = -V_N$.

The low R_o of the DUT resulted in a too low output signal that could not accurately be measured by the VNA for $f \leq 0.5$GHz. Therefore, for $f \leq 0.5$GHz, a Signal Generator (SG) (Agilent E8267D-544) and a Signal Analyser (SA) (Agilent N9030A) with a lower noise floor were used. The used GSG RF probe and cables were first characterized with a VNA and de-embedded from the measurements along with the VCSEL. The on-chip capacitance was not de-embedded for these low frequencies.

V. RESULTS AND DISCUSSION

A. I-V RETICLE MEASUREMENTS

The measured I-V characteristics (or Gummel plots) of five PIN-diodes with varying L_C located on one reticle are shown in Fig. 5. Here $V_{BG} = V_{BG,max,R}$ (obtained from optical measurements as discussed further in this section). Based on the exponential relation between I_D and V_{PN} ($V_{PN} > 0$V) it can be concluded that the diodes are electrically functional.

The forward characteristics, *i.e.,* for $V_{PN} > 0$, indicate an increased series resistance for larger L_C, suggesting that a longer resistive intrinsic region limits the maximum current.

L_C also influences the slopes of the forward characteristics, expressed in ideality factor (η), which is calculated from (a fit of) the measured current (I_D) using the Shockley equation [20]:

$$I_D = I_{sat}\left(e^{\frac{V_{PN}}{\eta V_T}} - 1\right) \tag{1}$$

where I_{sat} is the saturation current, $V_T = kT/q$ is the thermal voltage (equal to 25.9mV at room temperature), k is Boltzmann's constant, T is the temperature, and q is the elementary charge.

According to theory, for the V_{PN} range in which the SRH recombination current is dominant, η should be equal to 2 [20]. This, together with I_{sat}, is related to the SRH recombination rate which can be expressed as [20], [21]:

$$R_{SRH} \approx \frac{pn}{\tau_{SRH}(n + p + 2n_i)}, \tag{2}$$

where p is the hole concentration, n is the electron concentration, n_i is the intrinsic carrier concentration and τ_{SRH} is the (effective) SRH recombination lifetime (assuming the hole lifetime equals the electron lifetime). The SRH

recombination is most efficient in the regions where p is equal to n and the pn product is maximal [21]. For PIN-diodes this is the case in the intrinsic region.

From the measured forward characteristics it was found that η is not equal to 2 for the V_{PN} regime where the recombination current is expected to dominate. Instead, a steady increase of η as a function of V_{PN} for $V_{PN} > 0.2$V can be seen, followed by an abrupt decrease. Its maximum value increases with increasing L_C and tends to occur at $V_{PN} \approx 0.6$V. This dependency of η on both V_{PN} and L_C can be explained by the fact that L_C is reduced by finite Debye lengths as mentioned in Section II. The resultant reduction of the intrinsic volume lowers the recombination current. Below a certain L_C, this effect causes the PIN-diode to act like a PN-diode.

For longer devices, as V_{PN} is increased, the quasi-Fermi levels split more, and the potential barrier between V_P and V_N lowers, thus more charge is injected into the intrinsic region. The lengths of the transition tails between the intrinsic region and n^+ as well as p^+ also reduce, increasing $L_{C,eff}$ which translates to the increase of the intrinsic volume. This causes the saturation current of the diode (I_{sat}) to be V_{PN}-dependent and is visible in the Gummel plots as an increase of η. At a certain point the resultant $L_{C,eff} \approx L_C$. In this situation, the I_{sat} of the recombination current saturates at its maximum value. Then η reaches its peak value and ideally settles at 2.

For $V_{PN} > 0.6$V, diffusion starts to dominate due to the injection of minority carriers into p^+ and n^+, which is exponentially dependent on V_{PN}. Since η should be unity when diffusion currents dominate, a sudden drop in η can be observed for $L_C \leq 1090$nm for that V_{PN} range.

At relatively high current densities, series resistance reduces the slope of I_D, which translates to an increase in η. As can be observed in the figure, the series resistance for maximum L_C (2127nm) is so large that it precedes the onset of the diffusion current so that η does not first bend towards unity after reaching 2. Instead, it keeps increasing. The abnormally large η values visible in Fig. 5 and the probable cause is elaborated on in Section V.C.

Fig. 6 shows the maximum recombination current per unit width ($I_{sat,max}/W_C$) as a function of L_C. Here V_{BG} is set to $V_{BG,max,rec}$, which is defined as the V_{BG} for which there is maximum recombination current (η is close to 2) for a given V_P and V_N. $V_{BG,max,rec}$ should not be confused with $V_{BG,max,R}$. The saturation current was calculated using Eq. (1) with the measured I_D and the assumption that $\eta = 2$.

In the figure, the measurements for four different reticles are presented. The standard deviation is shown with error bars. The average $I_{sat,max}/W_C$ seems to increase linearly with L_C up to 527nm. An increase in L_C translates to a linear increase of the volume where recombination takes place (*i.e.,* intrinsic region) assuming a fixed charge carrier density. Thus there is a linear relation between I_{sat} and L_C, until L_C approaches or exceeds the diffusion length:

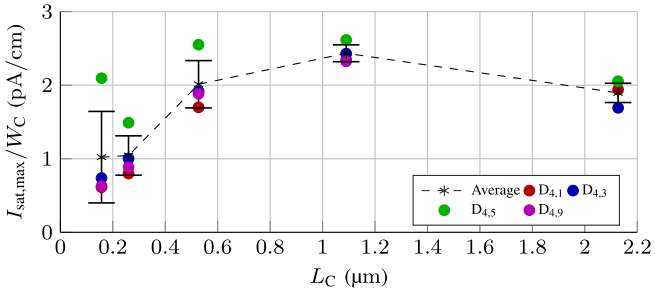


FIGURE 6. $I_{sat,max}/W_C$ against L_C on wafer B for $V_{PN} = 0.2$V, $V_{BG} = V_{BG,max,rec}$, and $V_P = -V_N$.

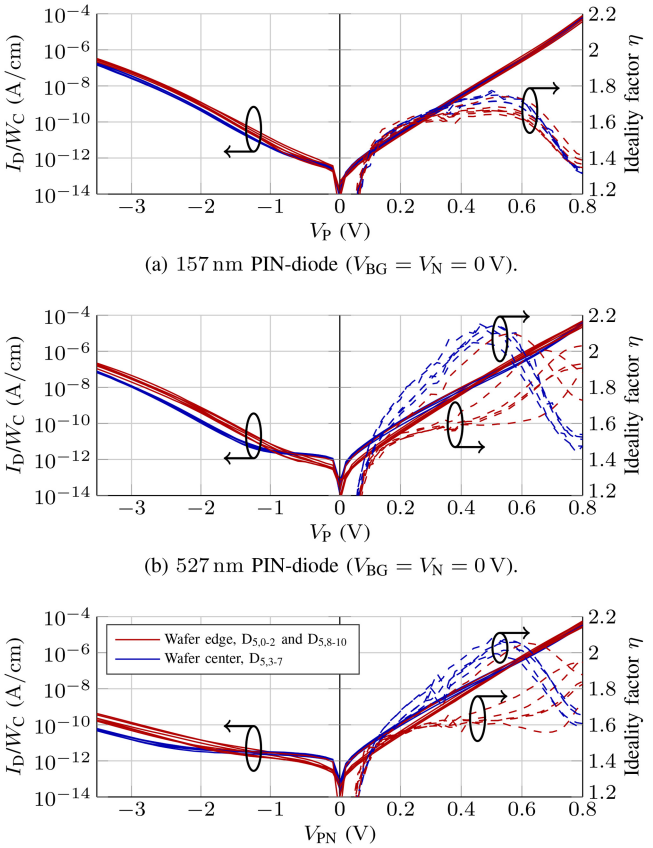
then significantly more carriers recombine before they reach the p^+ or n^+ regions. This results in a deviation from the linear dependence, as seen for devices longer than 527nm. First $I_{sat,max}/W_C$ starts to saturate for the 1090nm devices, and finally decreases for the 2127nm devices. Note that the diffusion length depends on both the interface quality and SOI quality. It is expected that the diffusion lengths of 22FDX® will be in the same order of magnitude as the diffusion lengths of the 28nm FDSOI process reported by Lee et al. [24], where a minority carrier lifetime (τ_{eff}) of 5-10ns was found, suggesting a hole diffusion length of ~300nm. Thus in the case of the 2127nm device, the pn product has reduced in a large portion of the intrinsic region.

B. I-V WAFER MEASUREMENTS

Fig. 7 shows the measured I-V characteristics (Gummel plots) with ideality factors of PIN-diodes across an entire row on wafer A. In Fig. 7(a) and 7(b) $V_{BG} = V_N = 0$V and anode potential V_P is swept. PIN-diodes on reticles closer to the edge of the wafer, $D_{5,0\text{-}2}$ and $D_{5,8\text{-}10}$ (Fig. 8), have higher currents when reverse biased. This is especially visible for the devices with L_C equal to 527nm.

Based on conventional bulk diode behaviour, the reverse bias current is expected to be more or less constant before going into avalanche [20]. However, Fig. 7 shows a significant increase in current for stronger reverse bias. This is likely caused by additional conduction paths or trap-assisted tunnelling as indicated by the different back-gate potential dependencies in Fig. 7(b) and 7(c). As discussed in Section II, tunnel junctions can be formed when a high V_{BG} is applied which, combined with traps caused by local defects, results in trap-assisted tunnelling. On top of that, due to the asymmetry in the devices (doping or work function differences) tunnel junctions may have already formed for $V_{BG} = 0$V.

Fig. 7 shows that the 527nm devices have a higher η than the 157nm devices. The highest value for η on wafer A was found to be ~2.1 for the devices with L_C equal to 527nm. For the 157nm devices, the lower ideality factor is most likely due to the smaller lengths of their intrinsic regions and surface areas, which lowers the recombination current. In contrast, the diffusion currents are expected to be



(a) 157 nm PIN-diode ($V_{BG} = V_N = 0$ V).

(b) 527 nm PIN-diode ($V_{BG} = V_N = 0$ V).

(c) 527 nm PIN-diode ($V_{BG} = 0$ V and $V_P = -V_N$).

FIGURE 7. Gummel plots and calculated ideality factors of SOI PIN-diodes across wafer A for different back-gate (V_{BG}), anode (V_P), cathode (V_N) biasing, and physical length of the intrinsic region L_C. The curves corresponding to the reticles close to the edge of the wafer ($D_{5,0\text{-}2}$ and $D_{5,8\text{-}10}$) are red and those close to the centre ($D_{5,3\text{-}7}$) are blue. Note the different scale on the horizontal axis for positive and negative values.

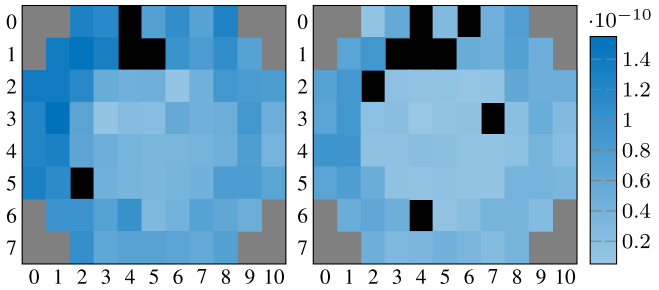


FIGURE 8. Wafer map showing I_D/W_C (A/cm) for the (left) 157nm and (right) 527nm devices on wafer A. Gray squares are outside of the wafer and black squares are samples that were accidentally destroyed in earlier measurements ($V_{BG} = V_N = 0$V and $V_P = -1.5$V).

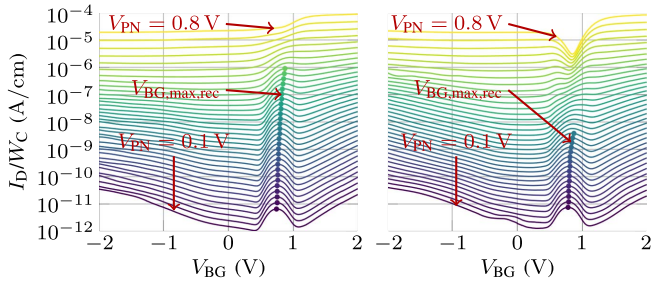


FIGURE 9. Diode current (I_D/W_C) against V_{BG} for varying V_{PN} (20mV steps), with $V_P = -V_N$ across wafer B. (left) $D_{4,3}$ with $L_C = 527$nm and (right) $D_{4,3}$ with $L_C = 2127$nm.

independent of L_C as long as L_C is much smaller than the diffusion lengths of the electrons and holes.

Differences between Fig. 7(b) and 7(c) in the currents and ideality factors stem from different biasing approaches. The asymmetric biasing in the former plot causes a significant increase in the reverse current and relatively large η values (above 2). Keeping $V_{BG} = V_N$ while sweeping V_P results in the intrinsic region effectively experiencing a changing potential difference between itself and the back-gate. As explained in Section II, the result is a dynamical change in electrostatic doping. An approach that mitigates this effect is symmetric biasing, implemented by forcing $V_P = -V_N$ as done for Fig. 7(c). This biasing method sets an almost static potential difference between the back-gate and the centre of the intrinsic region; this is used throughout Section V.C.

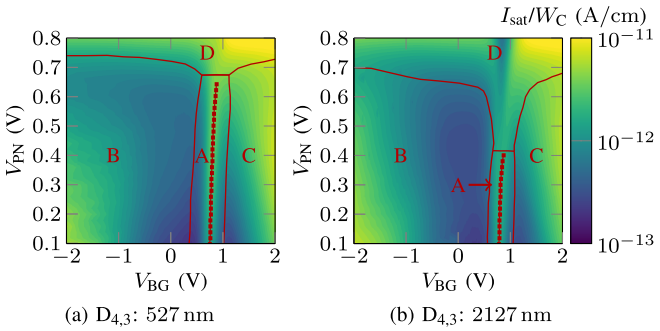
The Gummel plots in Fig. 7 show that the 527nm devices near the wafer edge have lower recombination currents, lower maximum η values, and reverse characteristics more similar to shorter devices. This likely suggests that the devices near the wafer edge have an effectively lower L_C than the devices in the centre.

Fig. 8 shows a wafer map of measured I_D/W_C of our 157nm (72 devices) and 527nm (68 devices) SOI PIN-diodes at $V_{BG} = V_N = 0$V and $V_P = -1.5$V. A clear circular pattern is observed, which stems from process-related factors, *e.g.*, the device processing or stress caused by the BEOL. In particular, the absolute current differences are less for shorter devices, indicating a dependency between L_C and location-dependent variations in the I-V curves. Such sensitivity to process-related aspects could be useful in PCM structures and general reliability monitoring.

C. I-V BACK-GATE CONTROL

Similar to earlier work [14], [17], Fig. 9 shows I_D/W_C as a function of V_{BG}, for V_{PN} between 0.1V to 0.8V. A change in V_{BG} modulates the carrier concentrations (n and p), which also changes R_{SRH} conform Eq. (2). This dependence yields maxima in the measured currents, at $V_{BG} = V_{BG,max,rec} \approx$ 0.8V. In Fig. 9 these maxima are marked by thick dots. At $V_{BG,max,rec}$, the intrinsic region has maximum volume and the diode behaves like a PIN-diode as explained in Section II.

Eq. (1) and the measurements shown in Fig. 9 are used to estimate I_{sat}, which is plotted as a function of V_{PN} and V_{BG} in Fig. 10. I_{sat} was chosen instead of I_D because it does not have an exponential dependence on V_{PN}, which helps in the visualization and analysis of the back-gate effect and its influence on the operation of the device. In these contour plots, four different regions can be identified. Region A corresponds to the PIN-diode operating region (conform



(a) $D_{4,3}$: 527 nm (b) $D_{4,3}$: 2127 nm

FIGURE 10. Contour plots of I_{sat}/W_C of the PIN-diode when sweeping V_{BG} and V_{PN} ($V_P = -V_N$), used to estimate $V_{BG,max,R}$.

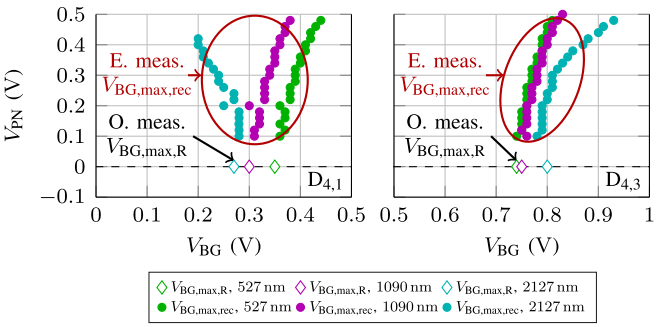


FIGURE 11. $V_{BG,max,rec}$ from electrical (E.) measurements (circles) compared to $V_{BG,max,R}$ from optical (O.) measurements (diamonds), (left) $D_{4,1}$ and (right) $D_{4,3}$ on wafer B.

Fig. 2(a)) where the recombination current is dominating and (close to) maximal, indicating intrinsic Si. The red markers are the $V_{BG,max,rec}$ for varying V_{PN}. Regions B and C correspond to the V_{BG} and V_{PN} range where the intrinsic region is electrostatically doped such that the diode behaves as a PN-diode (conform respectively Fig. 2(b) and 2(c)). Here the asymmetry between regions B and C is likely caused by differences in the epitaxially grown n^+/p^+ doped Si. Region D is where diffusion currents and/or series resistance dominate over the recombination current, obfuscating $V_{BG,max,rec}$.

Fig. 11 shows $V_{BG,max,rec}$ against V_{PN} as taken from the electrical measurements, and $V_{BG,max,R}$ acquired from the optical measurements for $V_{PN} = 0$V. It is shown that points located at ($V_{BG,max,rec}$, V_{PN}) converge to ($V_{BG,max,R}$, 0V). This occurs because as V_{PN} approaches 0V, the difference between $V_{BG,max,R}$ and $V_{BG,max,rec}$ is expected to decrease as both R_o and R_{SRH} are maximal when a PIN-diode with the largest possible intrinsic Si volume is electrostatically formed. Here results obtained from two different reticles are shown to illustrate how $V_{BG,max,rec} \approx V_{BG,max,R}$ for $V_{PN} \leq$ 0.2V.

Fig. 12 shows the difference between η for $V_{BG} = V_{BG,max,rec}$ and $V_{BG} = V_{BG,max,R}$, where $V_{BG,max,rec}$ is V_{PN} dependent and $V_{BG,max,R}$ is determined at $V_{PN} = 0$V. The devices do indeed behave more like PIN-diodes ($\eta =$

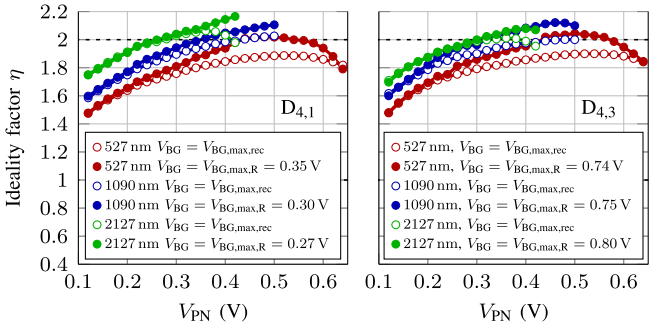


FIGURE 12. Calculated ideality factor (η) against V_{PN} for $V_{BG} = V_{BG,max,rec}$ and $V_{BG} = V_{BG,max,R}$, with $V_P = -V_N$, (left) $D_{4,1}$, and (right) $D_{4,3}$ on wafer B.

2) when they are optimally biased ($V_{BG} = V_{BG,max,rec}$). $V_{BG} = V_{BG,max,rec}$ can, for example, be supplied with a suitable (tracking) biasing circuit when a PIN-diode behaviour is required. This circuit would need to apply the average signal across the PIN-diode to the back-gate. The design of such a biasing circuit is beyond the scope of this paper.

The differences between the estimated $V_{BG,max,R}$ and the $V_{BG,max,rec}$ as acquired from optical measurements are shown in Fig. 13, and discussed in V.D.

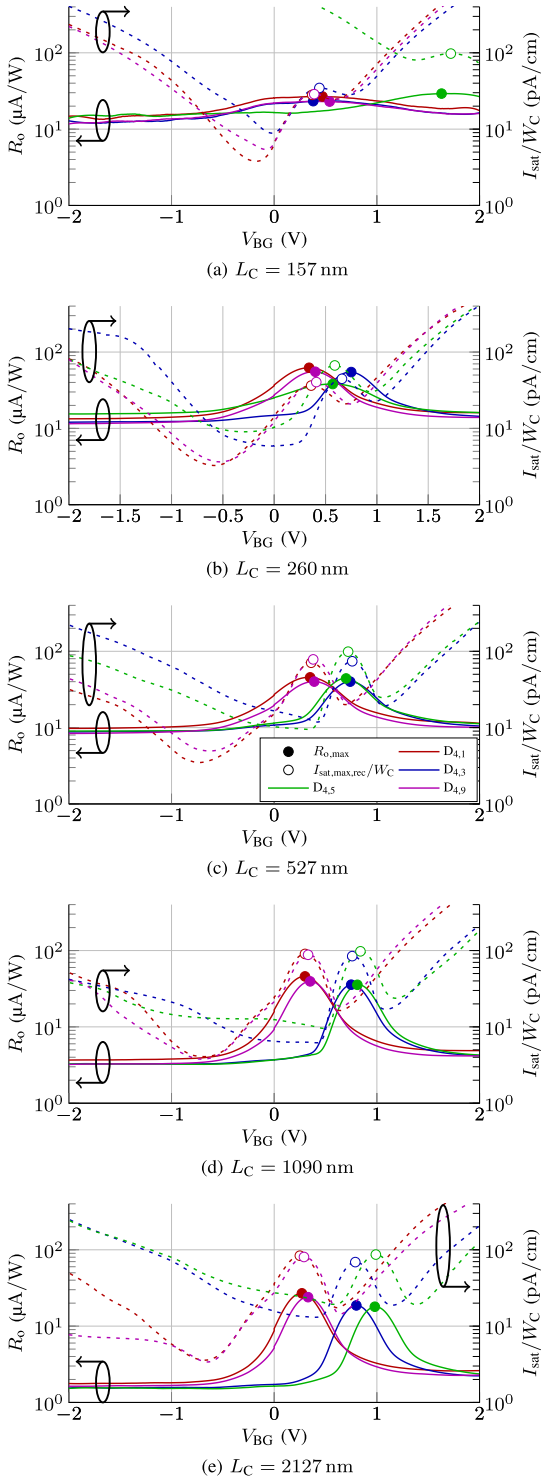
D. RESPONSIVITY MEASUREMENTS

The R_o is defined as the ratio of photocurrent and optical input power [25], [26]:

$$R_o = \frac{I_{PD}}{P_O} = \frac{q}{E_p}\eta_{EQE,PD}, \tag{3}$$

where I_{PD} is the photocurrent, P_O is the optical input power, E_p is the photon energy, and $\eta_{EQE,PD}$ is the external quantum efficiency. $\eta_{EQE,PD}(\propto \eta_F\eta_A)$ is the product of several ratios [26]: η_F ($\sim$0.72 [26]) is the fraction of P_O that is not reflected by the BEOL, and η_A is the fraction of optical power absorbed inside the PD. Using $\eta_A = 1 - e^{-\alpha_{oa} \cdot t_{Si}}$, with α_{oa} the absorption coefficient of Si at 850nm ($\alpha_{oa} \approx 0.04/\mu m$) [10] and t_{Si} is $\sim$6nm [12], $\eta_A = 2.4 \cdot 10^{-4}$. The ultra-thin SOI layer thickness in this technology limits the total percentage of absorbed light ($\sim$0.02% at 850nm when illuminated from above), which is significantly less in comparison to regular bulk devices [26]. Quantum confinement for $\sim$6nm t_{Si} will become significant (resulting in a different η_A and thus R_o), and trap-assisted recombination would result in a lower R_o, but to a first approximation these effects are neglected. Using these results $\eta_{EQE,PD}$ is calculated to be $1.5 \cdot 10^{-4}$ and thus R_o is expected to be in the order of 100μA/W.

Fig. 13 shows R_o versus V_{BG} of the PDs for devices with different L_C situated on four reticles on wafer B, with $V_{PN} = 0$V and a uniform illumination ($\sim 125 nW/\mu m^2$). R_o is maximal (62μA/W, in line with the simple first-order R_o calculation) at $V_{BG,max,R}$, where the device has the optimal electric field distribution (fastest electron-hole separation)



(a) $L_C = 157\,\text{nm}$
(b) $L_C = 260\,\text{nm}$
(c) $L_C = 527\,\text{nm}$
(d) $L_C = 1090\,\text{nm}$
(e) $L_C = 2127\,\text{nm}$

FIGURE 13. Responsivity measurements (solid curves) and I_{sat}/W_C (dashed curves) as a function of V_{BG} for various SOI PIN-diodes on four reticles and five different L_C. The R_o was obtained with $V_{PN} = 0V$ and uniform light (wavelength of 850nm and power density ~$125nW/\mu m^2$) across wafer B. I_{sat}/W_C was obtained with $V_{PN} = 0.2V$. The maximum values for both R_o ($R_{o,max}$) and I_{sat}/W_C ($I_{sat,max}/W_C$) have been indicated with markers.

and largest intrinsic Si volume size (largest amount of electron-hole generation). This R_o-dependence on V_{BG} has also been reported in [18].

TABLE 1. $V_{BG,max,R}$ and $V_{BG,max,rec}$ comparison and their effect on R_o and R_o/W_C

L_C (nm)	[1]$\lvert\Delta V_{BG}\rvert$		[1]Responsivity			
	[2]Avg. diff. (V)	[3]Std. dev. (V)	[4]Avg. $R_{o,max}$ (μA/W)	[4]Avg. $R_{o,max}/W_C$ (μA/(cm · W))	[5]Avg. diff. %	[3]Std. dev. %
157	0.10	0.03	26	274	0.40	0.34
260	0.04	0.03	53	730	2.17	2.72
527	0.02	0.01	42	836	0.45	0.24
1090	0.02	0.01	39	1322	0.40	0.41
2127	0.02	0.01	22	1292	0.16	0.19

[1] The averages (avg.) and standard (std.) deviations (dev.) are calculated for the $D_{4,1}$, $D_{4,3}$, $D_{4,5}$, $D_{4,7}$, and $D_{4,9}$ reticles on wafer B.
[2] $V_{BG,max,R}$ ($V_{PN} = 0\,V$) is obtained from optical and $V_{BG,max,rec}$ ($V_{PN} = 0.2\,V$) is obtained from electrical measurements. The absolute difference (diff.) is calculated between $V_{BG,max,R}$ and $V_{BG,max,rec}$.
[3] Standard deviation of the average difference.
[4] Average measured at $V_{BG} = V_{BG,max,R}$ and $V_{PN} = 0\,V$.
[5] Difference between $R_{o,max}$ and the R_o measured with $V_{BG} = V_{BG,max,rec}$ and $V_{PN} = 0\,V$. $V_{BG,max,rec}$ is determined at $V_{PN} = 0.2\,V$.

Fig. 13 also plots I_{sat}/W_C for $V_{PN} = 0.2V$ ($V_{PN} = 0V$ would result in $0A$ for purely electrical measurements). Near the I_{sat}/W_C and R_o maxima ($V_{BG} \approx V_{BG,max,R} \approx V_{BG,max,rec}$), the I_{sat}/W_C and R_o measurements have similar trends, indicating a direct correlation between the dependencies of I_{sat}/W_C and R_o on V_{BG}. For $V_{BG} \ll (V_{BG,max,R}, V_{BG,max,rec})$ and $V_{BG} \gg (V_{BG,max,R}, V_{BG,max,rec})$, an increase in I_{sat}/W_C can be observed, contrary to the R_o which slowly decreases. The increase in I_{sat}/W_C is likely due to the formation of tunnel junctions for the cases where a high concentration of carriers is present in the i-region as explained in Section II. For both I_{sat}/W_C and R_o, an actual PIN-diode has been electrostatically obtained at a $V_{BG}{=}V_{BG,max,R}{\approx}V_{BG,max,rec}$, which results in maximal SRH recombination current (at $V_{PN} > 0V$) and maximal photogeneration current (at $V_{PN} = 0V$).

Table 1 compares the optically measured $V_{BG,max,R}$ to the electrically measured $V_{BG,max,rec}$ ($V_{PN} = 0.2V$) for the L_C = 157nm, 260nm, 527nm, 1090nm, and 2127nm devices. The absolute difference between $V_{BG,max,R}$ and $V_{BG,max,rec}$ is between 10mV and 100mV (note that the used V_{BG} sweep step size during measurements is 10mV), thus proving that $V_{BG,max,rec}$ ($V_{PN} = 0.2V$) is a reasonable estimate for $V_{BG,max,R}$. This bias voltage also results in $R_o \approx R_{o,max}$. The maximum average $R_{o,max}$ was measured for the 260nm device ($53\mu A/W$). For the R_o normalized to W_C, the largest value was measured for the 1090nm device ($1322\mu A/(cm{\cdot}W)$).

In Fig. 14 the $R_{o,max}/W_C$ is plotted against L_C for various devices across wafer B. This curve shows an almost identical behaviour to the I_{sat}/W_C versus L_C curve also plotted in Fig. 6. It first increases linearly up to 1090nm because R_o/W_C is linearly dependent on L_C. Above 1090nm the R_o stops increasing, most probably due to a combination of phenomena related to the increased L_C, such as, *e.g.,* the reduction of the electric field across the diode and the L_C

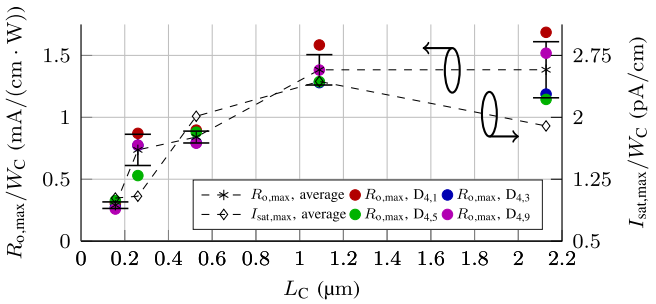


FIGURE 14. $R_{o,max}/W_C$ with $V_{BG} = V_{BG,max,R}$ and $V_N = V_P = 0V$ against L_C across wafer B. $I_{sat,max}/W_C$ with $V_{BG} = V_{BG,max,rec}$, $V_{PN} = 0.2V$, and $V_N = -V_P$ against L_C across wafer B.

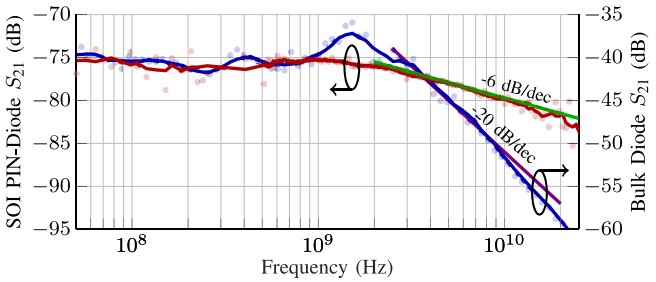


FIGURE 15. Frequency response of (left y-axis) the SOI PIN-diode with $L_C = 527nm$ (wafer A) and $V_{BG} = V_P = V_N = 0V$, and (right y-axis) a bulk (hybrid) PW/NW PD from [26] fabricated in the same technology with a diode bias voltage of 0V. The bulk diode is located on a separate die from a different wafer lot.

surpassing the diffusion lengths of the carriers inside the intrinsic region.

The SOI layer is located between two materials with a low dielectric constant, effectively forming a waveguide. Coupling light into this waveguide would be challenging due to the thickness of the BOX (20nm [12]) and Si film (∼6nm [12]), but if done properly, it would result in the light being absorbed along the lateral dimension of the back-gate controlled SOI PIN-diode with the possibility of improving R_o by orders of magnitude without losing any of the other benefits. That would open up (many) more optical applications for these PIN-diodes.

E. FREQUENCY RESPONSE

Fig. 15 shows the measured optical to electrical frequency response of both the SOI PIN-diode (wafer A) and a hybrid (bulk) NW/PW PD fabricated in the same technology [26].

The SOI PIN PD R_o is 62μA/W and the BW_{-3dB} and BW_{-6dB} are 5.9GHz and 15GHz, respectively. For comparison, the bulk NW/PW PD in the same technology for the same bias conditions has a R_o of 6mA/W and a BW_{-3dB} and BW_{-6dB} of 3.9GHz and 5.4GHz respectively [26]. Fig. 15 shows that the roll-off of the SOI PIN-diode is (much) less steep than for its hybrid counterpart. This better frequency response is likely due to the lower junction capacitance and larger depleted/intrinsic Si volume relative to the non-depleted/doped Si volume (where light can also be absorbed) of the SOI PIN PD compared to the bulk PD. This alleviates equalisation requirements and could be beneficial for (very) high bandwidth applications.

VI. CONCLUSION

Experimental back-gate controlled SOI PIN-diodes without a front-gate were fabricated as exploratory devices in a commercially available FDSOI technology, without requiring additional process steps. This means that these devices can be fabricated in any technology that uses a similar process. They are found to be functional, both electrically and optically. The measured responsivities at a wavelength of 850nm are $2 - 62\mu$A/W. The obtained BW_{-3dB} and BW_{-6dB} are 5.9GHz and 15GHz, respectively.

Electrostatic back-gate tuning shows a significant effect on the electrical characteristics and responsivity as predicted by theory. A method to estimate the optimal back-gate voltage for maximum responsivity solely based on electrical measurements has been proposed and demonstrated to be functional.

The presented SOI PIN-diodes open the way to new THz circuits, PCM structures, and optical applications, and enable new interfacing possibilities between the hybrid (bulk) and SOI layers via electrostatic interaction.

ACKNOWLEDGMENT

The authors would like to thank GlobalFoundries for providing silicon fabrication through the 22FDX university program. They also want to thank Jurriaan Schmitz and Bram Nauta (University of Twente) for the fruitful discussions and Luca Pirro and Michael Zier (GlobalFoundries) for helping with the 22FDX® technology aspects. Views and opinions expressed are however those of the authors only and do not necessarily reflect those of the European Union or the European Commission. Neither the European Union nor the European Commission can be held responsible for them.

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